In the Claims

Please amend claims 1 through 10, 12 14, 17 and 18 as follows:

1 (amended). A method for enabling a processor that directs I/O requests over a first communications channel to a first plurality of logical devices [and] during normal operations to switch and direct I/O requests over a second channel to a second plurality of logical devices normally operating as a mirror of the first plurality of logical devices [wherein] and each of the plurality of logical devices has an identifying control block [and the processor] , I/O requests normally [are] being processed using control blocks for the first plurality of logical devices, said method being responsive to a swap command to direct I/O requests to an identified logical device over the second channel and comprising the steps of:

A) determining, during normal operations, an operating validity of both the first and second pluralities of logical devices, and

B) [initiating] performing an address switch by:

i) verifying the operating validity of the logical devices in the first and second pluralities of logical devices corresponding to the identified logical device based upon the step of

determining operating validity during normal operations, and

ii) [exchanging] in response to a successful verification, blocking I/O requests to the identified logical device to enable the exchange of the information in each control block associated with the logical devices corresponding to the identified logical device in the first [plurality] and second pluralities of logical devices [with the information in each control block associated with the second plurality of logical devices], said blocking being terminated after the exchange whereby subsequent processor I/O requests to the identified logical device are directed to the corresponding logical device in the second plurality of logical devices.

2 (amended). A method as recited in claim 1 wherein said determination of operating validity of the first and second pluralities of logical devices occurs asynchronously and independently of said exchange of control block information for the identified logical device.

3 (amended). A method as recited in claim 2 wherein said determination <u>of operating validity of the first and second pluralities of logical devices</u> is made periodically <u>prior to said performing of said address switch with the identified logical device</u>.

4 (amended). A method as recited in claim 2 wherein the processor and logical devices can operate with different configurations and wherein said determination [responds] <u>of operating validity occurs in response</u> to a change in a configuration.

5 (amended). A method as recited in claim 2 wherein the processor and logical devices can operate in different operating modes, and wherein said determination [responds] <u>of operating validity occurs in response</u> to [the] <u>a</u> selected operating mode of the process with the first plurality of logical devices.

6 (amended). A method as recited in claim 2 wherein said determination includes a determination of <u>operating</u> validity for each of the first plurality of logical

devices and the corresponding logical device in the second plurality of logical devices.

7 (amended). A method as recited in claim 6 wherein a data structure includes a validity flag for each of the first plurality of logical devices and its corresponding one of the second plurality of logical devices and wherein said determination of operating validity sets the corresponding validity flag.

8 (amended). A method as recited in claim 7 wherein the swap command identifies at least one logical device and said blocking of I/O requests occurs with respect all of the identified logical devices in the first plurality of logical devices during the exchange of information [occurs while all the logical devices have been blocked for responding to any I/O request], said [block being released] unblocking occuring after all the exchanges are made whereby the redirection of processor I/O requests to the second plurality of logical devices occur essentially simultaneously thereby to produce a consistent transfer.

9 (amended). A method as recited in claim 7 wherein said exchange includes, for each identified logical device, the steps of:

i) selecting a single logical device in the first plurality of logical devices,

ii) blocking access to [that] the selected logical device,

iii) and thereafter exchanging the information in each control block associated with the selected [one of the first plurality of logical devices] logical device and the corresponding [of] logical device in the second plurality of logical devices; and

iv) unblocking access to the selected logical [devices] device.

10 (amended). Apparatus for enabling a processor that directs I/O requests over a first communications channel to a first plurality of logical devices and to switch and direct I/O requests over a second channel to a second plurality of logical devices normally operating as a mirror of the first plurality of logical devices in response to a swap command that identifies a logical device in the first plurality of logical devices wherein

each of the plurality of logical devices has an identifying control block and the processor I/O requests normally are processed using control blocks for the first plurality of logical devices, said [method] apparatus comprising:

A) means for determining, during normal operations, an operating validity of the first and second pluralities of logical devices,

B) means for initiating an address switch including:

i) means for verifying the operating validity of the logical devices in the first and second pluralities of logical devices corresponding to the identified logical device, and

ii) means responsive to the verification for [exchanging] blocking I/O requests to the identified logical device to enable the exchange of the information in each control block associated with the logical devices in the first [plurality] and second pluralities of logical devices [with the information in each control block associated with the second plurality of logical devices] corresponding to the identified logical device, said blocking being terminated when the exchange is complete whereby subsequent

processor I/O requests with the identified logical device are directed to the corresponding logical device in the second plurality of logical devices.

11 (original). Apparatus as recited in claim 10 additionally comprising means for activating said determination means asynchronously and independently of the operation of said exchange means.

12 (amended). Apparatus as recited in claim 11 additionally comprising means for activating said determination periodically prior to the operation of said address switching means.

13 (original). Apparatus as recited in claim 11 wherein the processor and logical devices can operate with different configurations and wherein said apparatus additionally comprises means for activating said determination means in response to a configuration change.

14 (amended). Apparatus as recited in claim 11 wherein the processor and logical devices can operate in different operating modes, and wherein said apparatus additionally

comprises means for activating said determination means in response to [the] a selected operating mode of the process with the first plurality of logical devices.

15 (original). Apparatus as recited in claim 11 wherein said determination means includes means for determining the validity for each of the first plurality of logical devices and the corresponding logical device in the second plurality of logical devices.

16 (original). Apparatus as recited in claim 15 additionally comprising a data structure including a validity flag for each of the first plurality of logical devices and its corresponding one of the second plurality of logical devices, said determination means sets the corresponding validity flag if valid operating conditions exist.

17 (amended). Apparatus as recited in claim 16 wherein the swap command identifies at least one logical device, said apparatus additionally comprising means for blocking access to all the identified logical devices before the information exchanges and means for releasing said blocking means after all the exchanges are made whereby the redirection of processor I/O requests to the second

plurality of logical devices occur essentially simultaneously and consistently.

18 (amended). Apparatus as recited in claim 16 wherein said exchange means includes:

i) means for selecting a single logical device in the first plurality of logical devices,

ii) means for blocking access to [that] selected logical device, said exchange means being activated in response to said blocking means, and

iii) means for releasing said unblocking means.